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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,476	01/23/2004	Naoto Shiraishi	247973US2	4925
22850	7590	03/18/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			CASCHERA, ANTONIO A	
			ART UNIT	PAPER NUMBER
			2676	

DATE MAILED: 03/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b> 10/762,476	<b>Applicant(s)</b> SHIRAISHI, NAOTO	
	<b>Examiner</b> Antonio A' Caschera	<b>Art Unit</b> 2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

#### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.  
     4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5, 7-14, 16-23 and 25-27 is/are rejected.
- 7) ☒ Claim(s) 6, 15 and 24 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 23 January 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
     a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____. |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>4/23/2004</u> . | 6) <input type="checkbox"/> Other: ____.  |

## DETAILED ACTION

### *Priority*

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in the pending application.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1, 10 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Iida et al. (U.S. Patent 6,473,091 B1).

In reference to claims 1, 10 and 19, Iida et al. discloses an image processing apparatus and method for performing blending and dithering techniques (see column 1, lines 8-10). Iida et al. discloses the processing apparatus to comprise of a computer graphics system, further made up of a main processor, main memory, I/O interface and rendering circuitry (see column 5, lines 24-26 and 40-43). Iida et al. discloses the main processor, acting as a command analyzing unit, by obtaining color information of graphic data from main memory, in accordance with a software application, and performing various geometrical processing to generate polygon rendering data (see column 5, lines

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46-50). Iida et al. further discloses the polygon rendering data to include data making up triangle or polygon vertices, the vertices defined by xyz and RGB color type data, along with others (see column 5, lines 57-64). Note, the office interprets the command analyzing unit of applicant's claim functionally equivalent to the main processor of Iida et al. Iida et al. also discloses the polygon data being passed on to the rendering unit (see column 5, lines 53-56), wherein the rendering unit comprises a DDA setup circuit, a triangle DDA circuit, a texture engine circuit and a CRT control circuit, along with other circuitry (see column 6, lines 14-18). Iida et al. discloses the combination of the DDA setup circuit and triangle DDA circuit to obtain color information of scanned pixel points within the polygon through interpolation in unit-length movement (see columns 6-7, lines 60-6, column 7, lines 53-56 and columns 7-8, lines 65-3). Iida et al. also discloses color data (RGB data) to be calculated for each pixel inside the polygon or triangle (see column 7, lines 49-52) which the office interprets equivalent to producing the color information for an entirety of the object, of applicant's claims. Note, the office interprets the combination of DDA setup and triangle DDA circuits functionally equivalent to the drawing unit of applicant's claim. Iida et al. discloses the texture engine blending DDA calculated pixel data with pixel data read from memory and outputs these blending values to another memory unit (see column 10, lines 32-40), the texture engine is interpreted as functionally equivalent to the image processing unit of applicant's claim. Further, in reference to claim 19, Iida et al. discloses the above described apparatus and method to be applied to computer aided design systems and amusement machines (see column 1, lines 12-13) both implementing some sort of computer to execute calculations therefore, the office interprets the invention of Iida et al. to inherently disclose an image processing

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program since readable-instructions, programs or computer code are inherent in computers.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 2-5, 11-14 and 20-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al. (U.S. Patent 6,473,091 B1) in view of Levison (U.S. Patent 6,008,815).

In reference to claims 2, 11 and 20, Iida et al. discloses all of the claim limitations as applied to claims 1, 10 and 19 respectively above in addition, Iida et al. discloses the DDA setup circuit performing a setup operation whereby the difference of a side of the triangle from a horizontal direction is obtained for RGB color data (see column 6, lines 60-67). Iida et al. also discloses the DDA setup circuit calculating start and end points on a left/right side of a triangle, the points lying on a horizontal line (see column 7, lines 1-4 and 22-42). Note, the office interprets the DDA setup circuitry of Iida et al. functionally equivalent to the setup unit and start point unit of applicant's claim. Iida et al. discloses the triangle DDA circuitry to interpolate color data along the horizontal line in accordance with x and y coordinates of the start point and color data of the start point (see column 7, lines 53-56, columns 7-8, lines 65-3, column 8, lines 11-23 and line

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segment BD, defined in xy space of Figure 2). Iida et al. does not explicitly disclose a plane equation of the object with respect to the color information of each endpoint however Levison does. Levison discloses a method for polygon rendering for use in 3D computer graphics whereby color difference data is calculated using a plane equation which includes endpoint data (see column 1, lines 6-7, columns 5-6, lines 51-37 and  $(x_s, y_i)$ ,  $(r_s, g_s, b_s, z_s)$ ,  $(x_e, y_i)$  and  $(r_i, g_i, b_i, z_i)$  of Figure 4). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the polygon rendering techniques using plane equations of Levison with the image processing techniques of Iida et al. in order to provide a method of polygon rendering in which the required number of processing cycles is reduced thereby accelerating interpolation processes (see column 1, lines 36-39 of Levison).

In reference to claims, 3, 12 and 21, Iida et al. and Levison disclose all of the claim limitations as applied to claims 2, 11 and 20 respectively above in addition, Iida et al. discloses the DDA setup circuit to calculate the change of values between starting and endpoints, these values include color data changes (see columns 6-7, lines 60-4). Note, since Iida et al. discloses calculating the difference of a side of the triangle for color data (see column 6, lines 64-67), the office interprets that Iida et al. inherently discloses computing color information corresponding to each endpoint. Further, since Iida et al. discloses giving identical functions to a plurality of modules in parallel to perform processing, thereby creating a more efficient system (see column 4, lines 20-22), the office interprets that Iida et al. inherently discloses computing such color information in parallel in order to create more efficiency in the system.

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In reference to claims 4, 13 and 22, Iida et al. and Levison disclose all of the claim limitations as applied to claims 2, 11 and 20 respectively above in addition, Iida et al. discloses the DDA setup circuit to calculate the x coordinate with respect to a displacement in the y-direction of a side of the triangle first when drawing a horizontal line from left to right, the line based upon start and end points (see column 7, lines 1-4 and 27-30). Iida et al. also discloses the triangle DDA circuit to interpolate color data of all pixels within the triangle based upon DDA setup circuit "change data" (see column 7, lines 49-56). Note, since Iida et al. discloses that the triangle DDA circuit interpolates color data in all pixels within the triangle based upon "change data" derived from the DDA setup circuit, which in turn uses start and end point data for computing "change data," the office interprets that Iida et al. inherently discloses interpolating color information in a vertical direction as pixels within the triangle are located at various y values and these pixels are interpolated. Further note, the office interprets the DDA setup and triangle DDA circuits of Iida et al. functionally equivalent to the vertical x value interpolating unit and vertical color information interpolating unit, respectively, of applicant's claim.

In reference to claims 5, 14 and 23, Iida et al. and Levison disclose all of the claim limitations as applied to claims 2, 11 and 20 respectively above. Iida et al. discloses the triangle DDA circuitry to interpolate color data along the horizontal line in accordance with x and y coordinates of the start point and color data of the start point (see column 7, lines 53-56, columns 7-8, lines 65-3, column 8, lines 11-23 and line segment BD, defined in xy space of Figure 2). Further, since Iida et al. discloses giving identical functions to a plurality of modules in parallel to perform processing, thereby

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creating a more efficient system (see column 4, lines 20-22), the office interprets that Iida et al. inherently discloses computing such color information in parallel in order to create more efficiency in the system.

4. Claims 7-9, 16-18 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Iida et al. (U.S. Patent 6,473,091 B1) in view of Weed (U.S. Patent 6,809,740 B1).

In reference to claims 7, 16 and 25, Iida et al. discloses all of the claim limitations as applied to claims 1, 10 and 19 respectively above. Iida et al. does not explicitly disclose converting color information however Weed does. Weed discloses a method of mapping data by quantizing samples and accessing a lookup table such that the average of the output data for a neighborhood of samples converges to a result that is comparable to an interpolated result (see column 1, lines 8-15). Weed discloses a color conversion module for receiving graphics data including color information and performing the actual conversion of colors from one color space to another (see column 9, lines 30-40 and #114 of Figure 5). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the color conversion techniques of Weed with the image processing techniques of Iida et al. in order to create a more portable system, allowing for the system to accept and process many different color signals therefore providing compatibility between devices such as printers and computing devices (see column 1, lines 17-25 of Weed).

In reference to claims 8, 17 and 26, Iida et al. and Weed disclose all of the claim limitations as applied to claims 7, 16 and 25 respectively above in addition, Weed discloses a dithering process whereby a selected number of bits from a sample remains



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after truncation using a mask array (see column 5, lines 4-6 and 44-53). Weed also discloses the color conversion module to perform such dithering processes by using the mask array to index a lookup table holding quantized color data (see column 9, lines 35-50). Note, the office interprets the color conversion module of Iida et al. functionally equivalent to the halftone unit of applicant's claim.

In reference to claims 9, 18 and 27, Iida et al. and Weed disclose all of the claim limitations as applied to claims 8, 17 and 26 respectively above in addition, Weed discloses quantizing the color data so that only the most significant bits of sample color data are used to represent the color data (see column 12, lines 12-26). For example, Weed discloses using the four most significant bits to represent RGB data (see Figure 8B). Weed also discloses transferring dithered and quantized data to a queue manager for storage of the color data associated with each pixel to be output (see column 9, lines 60-64). Note, the office interprets the color conversion model to perform functionally equivalent to the fixed length data generation unit of applicant's claim as the dithered data of Weed is truncated to a fixed number of most significant bits.

#### ***Allowable Subject Matter***

5. Claims 6, 15 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

In reference to claims 6, 15 and 24, the prior art of record (Iida et al. (U.S. Patent 6,473,091 B1), Levison (U.S. Patent 6,008,815) and Weed (U.S. Patent 6,809,740 B1)) does not explicitly disclose controlling a change of color by interpolating color in

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horizontal and vertical directions, in accordance with a mesh shaped like a square, surround the object and divided into minimal color lengths in vertical and horizontal directions.

### ***References Cited***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

- a. Shiraishi (U.S. Patent 5,502,802)
  - Shiraishi discloses a polygonal image-drawing processor providing a direction of a linear vector on each of the sides of a polygon based on information about two end points.
- b. Omori (U.S. Patent 5,977,984)
  - Omori discloses a rendering apparatus and method which converts apex data of a polygon in a 3D space into data in a display coordinate system.
- c. Taylor et al. (U.S. Patent 6,433,790 B1)
  - Taylor et al. discloses a method and system for rendering a feature for display on an array of pixels by expanding the feature into a polygon.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Antonio Caschera whose telephone number is (571) 272-

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7781. The examiner can normally be reached Monday-Thursday and alternate Fridays between 7:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella, can be reached at (571) 272-7778.

**Any response to this action should be mailed to:**

Commissioner of Patents and Trademarks

Washington, D.C. 20231

**or faxed to:**

**(703) 872-9314 (for Technology Center 2600 only)**

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.



MATTHEW C. BELLA  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600

aac

3/8/05